REMARKS / ARGUMENTS

Claims 21, 23-25, 27, 29-39, and 44-55 remain pending in this application. No claims have been canceled without prejudice or disclaimer. New claim 55 been added.

Double Patenting Rejection

Claims 21, 23-25, 27, 29-39 and 44-54 are pending and stand provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 21-25, 33, 35, 37-42, 57 and 58 of co-pending Application No. 11/031,556. Without admitting to the propriety of the rejection, Applicants submit herewith a terminal disclaimer to avoid the rejection.

35 U.S.C. § 103

Claims 21-28 and 30-52 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hubis et al (U.S. Patent No. 6,343,324) in view of Klein (U.S. Patent No. 6,108,732) and Yamamoto et al (U.S. Pub. No. 2001/0023463). Claim 29 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hubis et al, in view of Klein and Yamamoto et al, as applied to claim 21, and further in view of Kuchta at al (U.S. Patent No. 6,014,319). Claims 53 and 54 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hubis et al in view of Klein, Yamamoto et al and Matsunami et al (U.S. Pub. No. 2002/0091898). These rejections are traversed as follows.

Claim 21, for example, has been amended to clarify that the second interface adaptors are coupled to a plurality of disk drives and receive data stored in a cache memory adaptor based on third control information sent from at least one processor asynchronously with receipt of a write request at said first interface adaptors and store data in the disk drives. The first interface adaptors are recited to be coupled to at least one host computer. Claim 21 recites that the number of processor adaptors is increased or decreased independently of the first and second interface adaptors, the cache memory adaptor and a switch adaptor, based on required performance. Claim 21 has also been amended to recite that the processor adaptors can access to each of the first and second interface adaptors. Claim 21 has been further amended to recite that based on the processing load of the first interface adaptors which are coupled to the at least one host computer and the processing load of the second interface adaptors which are coupled to the plurality of disk drives, the number of processors is allocated to the first and second processing load, accordingly. In other words, the interface adaptors of the first and second interface adaptors that have the greater processing load have a larger number of processors allocated thereto. Similar amendments have been made to the remaining independent claims.

None of the cited references disclose or suggest these features of the presently claimed invention. Hubis et al disclose a basic structure of a storage system. Hubis et al do not disclose a plurality processor adaptors or that the number of processor adaptors are increased or decreased independently based on required performance as recited. The Examiner relies upon Klein for curing this deficiency. However, the combination of Hubis et al and Klein, at a minimum, do not disclose

that the processor adaptors have a plurality of processors, each assigned to operate according to processing loads as previously recited in the claims.

The Examiner now attempts to rely upon Yamamoto et al for curing the deficiencies in Hubis et al and Klein. Yamamoto et al disclose that a controller is implemented by a number of individual processor elements in order to provide parallel processing so that multiple different processes can be running simultaneously (see [0020]). However, the microprocessors running multiple processes in parallel are used for handling the transfer of data in response to read requests issued by the host systems 12 (see Fig. 1 and [0033]).

On the other hand, with respect to performing I/O requests to the physical storage 14 in Yamamoto, it is first determined in step 84 of Fig. 5 whether the data is contained in the memory/cache unit 22. If not, the request is passed to a load distribution process as shown in step 87. This load distribution process is shown in various embodiments in Figs. 9-11. Fig. 9 discloses a load distribution process 120 which uses priorities or a "round-robin" technique (see [0039]). An alternate load distribution process 130, as shown in Fig. 10, a physical disk unit having the lowest processing request, will be selected (see [0043]). Finally, in load distribution process 150, as shown in Fig. 11, it is determined whether a physical disk has a load within a load condition parameter (see [0048] and [0049]).

Therefore, Yamamoto et al do not disclose or suggest a plurality of processors that are allocated based on the load of first interface adaptors which are coupled to at least one host computer and a load of second interface adaptors which are coupled to a plurality of disk drives and performing processing asynchronously with

processing performed by the first interface adaptors. In other words, according to the presently claimed invention, based on the processing loads of the first interface adapters which are coupled to at least one host computer and the second interface adaptors which are coupled to a plurality of disk drives and performing processing asynchronously with processing performed by the first interface adaptors, respectively, the number of processors is appropriately allocated to the first and second interface adaptors.

The deficiencies in Hubis et al, Klein and Yamamoto et al are not overcome by resort to Kuchta at al or Matsunami et al, which are attempted to be used to reject dependent claims 29, 53 and 54. However, at a minimum, Kuchta et al and Matsunami et al do not cure the above-mentioned deficiencies of Hubis et al, Klein and Yamamoto et al with respect to the independent claims. As such, it is submitted that the pending claims patentably define the present invention over the cited art.

Conclusion

In view of the foregoing, Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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